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| EWULogo.png | | **EAST WEST UNIVERSITY** | | |
| **Department of Computer Science and Engineering** | | |
| **B.Sc. in Computer Science and Engineering Program** | | |
| **Final Examination, Summer 2020** | | |
| **Course:** | | **CSE360 – Computer Architecture, Section 3** | | |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Associate Professor, CSE Department** | | |
| **Full Marks:** | | **25** | | |
| **Exam Time:** | | **1 Hour 20 Minutes** | **Submission Time: 10 Minutes** | |
| **Note:** There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin. | | | | |
| 1. | Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes five bus clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers one byte of information between memory and I/O devices   1. Suppose we clock the 8237A at a rate of 8MHz. How long does it take to transfer one byte? 2. What would be the maximum attainable data transfer rate? 3. Assume that the memory is not fast enough and we have to insert three wait states per DMA cycle. What will be the actual data transfer rate? | | | [ CO2, C3, Mark: 1+1+1= 3] |
| 2. | A 64-bit computer has three selector channels and two multiplexor channels. Each selector channel supports four magnetic disk and three magnetic tape units. The multiplexor channel has one line printer, two card readers, and 13 VDT terminals connected to it. Assume the following transfer rate:  Disk drive: 830 Kbytes/sec  Magnetic tape drive 265 Kbytes/sec  Line printer 6.5 Kbytes /sec  Card reader: 1.2 Kbytes/sec  VDT: 1.1 Kbytes/sec  Estimate the maximum aggregate I/O transfer rate in this system. | | | [ CO2, C3, Mark: 3] |
| 3. | Analyze and Compare zero-, one-, two-, and three- address machines by writing programs to compute the following expression for each of the four machines.    The instructions available for use are as follows:   |  |  |  |  | | --- | --- | --- | --- | | 0 Address | 1 Address | 2 Address | 3 Address | | PUSH M  POP M  ADD  SUB  MUL  DIV | LOAD M  STORE M  ADD M  SUB M  MUL M  DIV M | MOV (X←Y)  ADD(X←X+Y)  SUB (X←X-Y)  MUL(X←X \*Y)  DIV(X←X/Y) | MOVE (X←Y)  ADD(X←Y+Z)  SUB(X←Y-Z)  MUL(X←Y\*Z)  DIV(X←Y/Z) | | | | [ CO3, C5, Mark: 5] |
| 4. | Convert the expression (A-B) \* (((C-D \* E)/F)/G) \* H to postfix notation using Dijkstra’s algorithm. Show the sequence of steps in the stack. | | | [CO3, C3, Mark: 4] |
| 5. | Consider a 16-bit processor in which the following appears in main memory, starting at location 230:   |  |  |  | | --- | --- | --- | | 230 | Load to AC | Mode | | 231 | 525 | | | 232 | Next instruction | |   The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 620. There is also a base register that contains the value 150. The value of 525 in location 231 may be part of the address calculation. Assume that location 298 contains the value 998, location 299 contains the value 999, and so on. Determine the effective address and the operand to be loaded for the following address modes.   1. Direct 2. Immediate 3. Indirect 4. PC relative 5. Displacement 6. Register 7. Register indirect 8. Autoindexing with increment, using R1 | | | [ CO4, C4, Mark: 6] |
| 6. | A nonpipelined processor has a clock rate of 2.9 GHz and an average CPI (Clock per instruction) of 5. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays the clock rate of the new processor has to be reduced to 2.3 GHz.   1. What is the speed up achieved for a program with 200 instructions? 2. What is the MIPS rate for each processor? | | | [CO4, C4 Mark: 2+2] |